Institute for Nuclear Research
National Academy of Sciences of Ukraine
HEP-TEC 2025

UNDERSTANDING, MODELING AND IMPLEMENTING THE ANALOGUE RESPONSE OF THE SILICON TRACKING SYSTEM OF THE CBM EXPERIMENT AT GSI/FAIR

O. Kshyvanskyi[1], V. Pugatch[1], M. Teklishyn[2]

[1] *Institute for Nuclear Research, National Academy of Sciences of Ukraine, Kyiv, Ukraine*
[2] *GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany*

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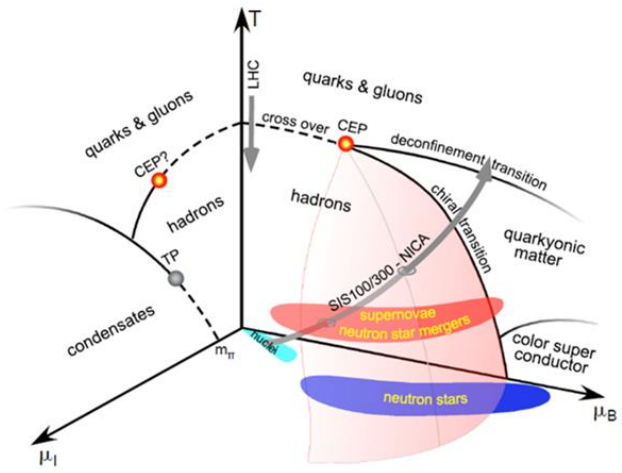
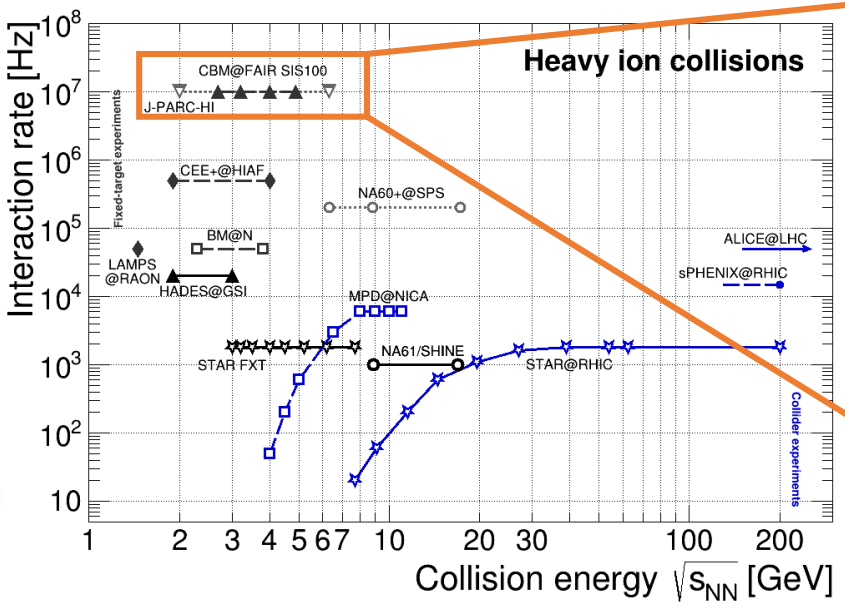
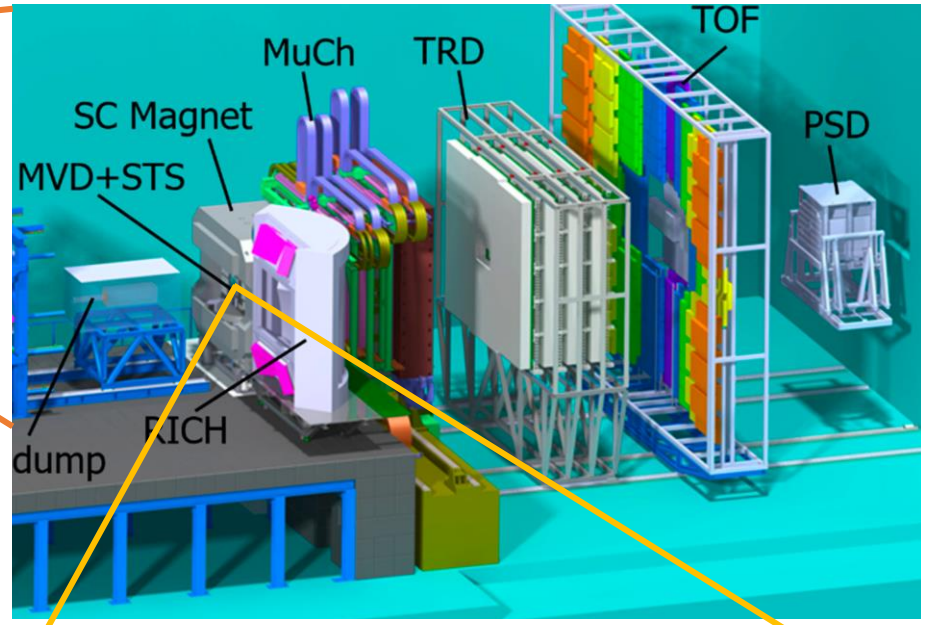
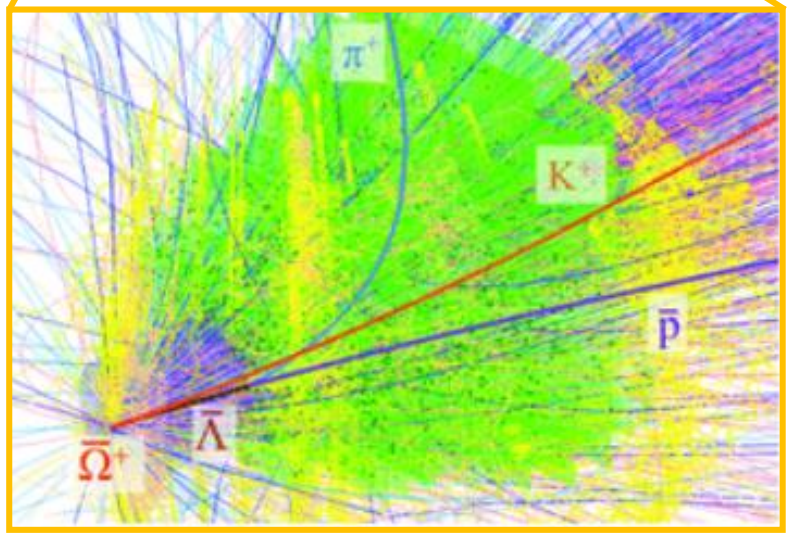
CBM experiment









Compressed Baryonic Matter (CBM) is a next-generation fixed-target experiment to be operated at GSI, FAIR (Facility for Antiproton and Ion Research), Darmstadt, Germany.

Heavy ion collisions:

- Rare probes and higher-order fluctuations,
- Beam-target interaction rate < 10 MHz,
- > 11 AGeV for Au, > 29 GeV for protons.

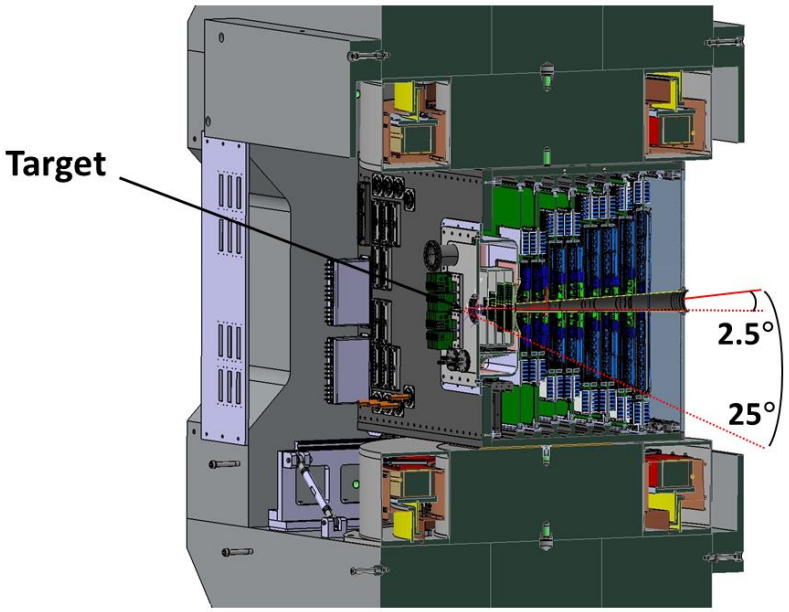
Investigation of the QCD phase diagram (observation of the phase transition and finding the critical point):

- Moderate temperatures.
- High baryon densities.

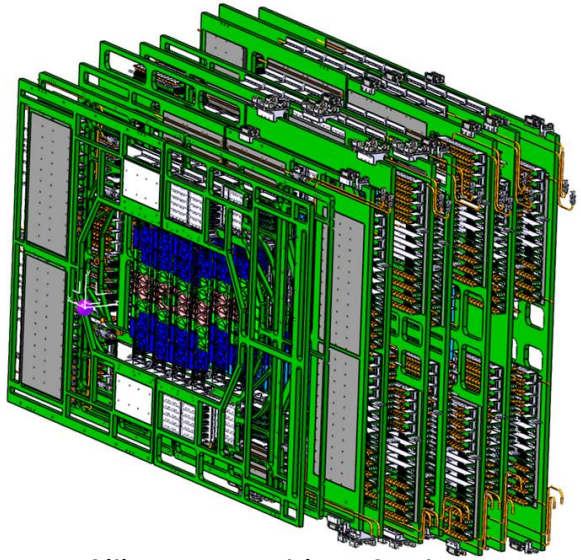
Silicon Tracking System

Silicon Tracking System (STS) – principal tracker of the CBM experiment:

- High track reconstruction efficiency (95% for p ≥ 1 GeV/c),
- Precise momentum resolution (1.5% for p ≥ 1 GeV/c),
- ≤ 700 particles per central Au + Au collision,
- Low momenta → low material budget (2 − 8% X_0),
- Continuous beam, free-streaming detector operation,
- **876 double-sided double-metal silicon micro-strip sensors, 8 tracking stations,**
- **Highly integrated objects: limited intervention after assembly.**



Silicon Tracking System installed inside the dipole magnet

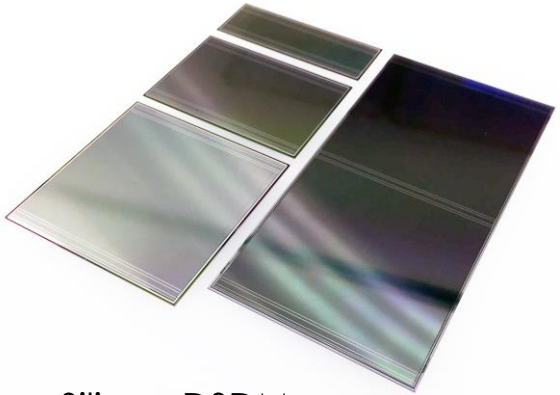

Silicon Tracking System

STS module design

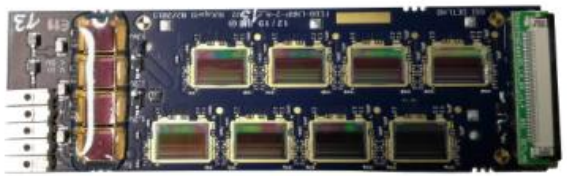
Detector module - functional building block of the STS, complex system with interconnected electrical properties. Main components:

- **Double-sided double-metal silicon sensor**
  - 1024 strips per side,
  - 320 µm thickness,
  - p-side tilted by 7.5° to the edge,
  - Width 62 mm, lengths 22, 42, 62 and 124 mm.
- **Two front-end boards (FEB)**
  - 8 custom-designed STS-XYTER (STS, X, Y coordinate, Time and Energy Read out) ASICs,
  - Power lines, voltage stabilizers (1.2 V and 1.8 V).
- **Ultra-thin micro-cables**
  - Length from 160 mm to 495 mm.

Prototype of the STS detector module



Silicon DSDM sensors



Prototype design of the FEB

Micro-cable

Electronic simulations of the STS module

- STS detector module is a **complex system** with **interconnected electrical properties**,
- STS is **a highly integrated object** with very limited access after assembly and installation.

Numerical simulations

- STS digitizer improvement,
- Improvement of the module quality control,
- Improvement of the reconstruction efficiency.

Electronic simulations of the STS module
Single-channel schematic

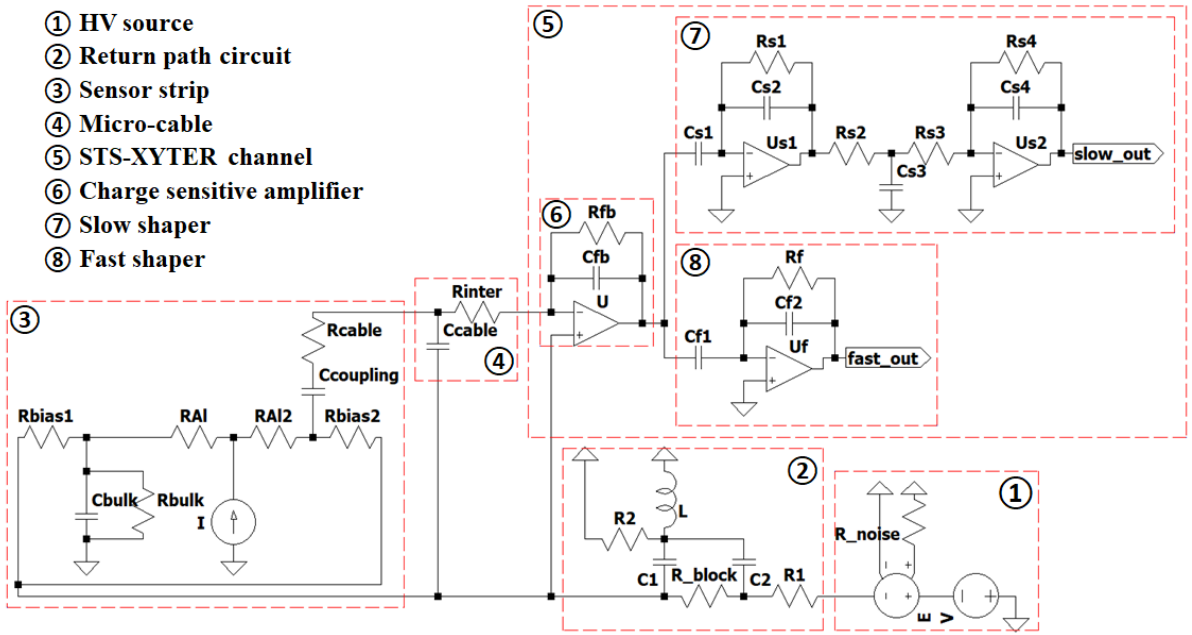
To perform simulations **LTSpice** (analog electronic circuit simulator) is used.

- Free software.
- No limitations on the number of components and subcircuits.
- Includes exhaustive library of possible components.
- Allows to create custom components.

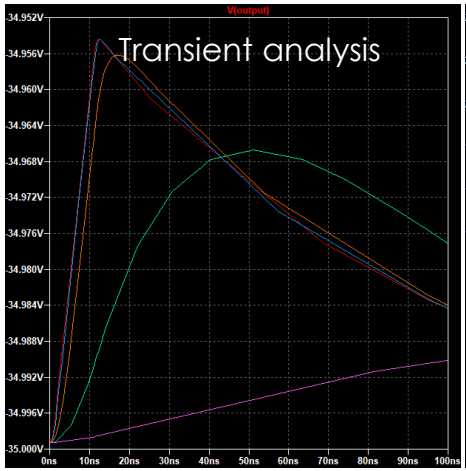
Start with a simplified schematic of a **detector with a single channel**, and gradually increase the complexity of the schematic to account for various effects.

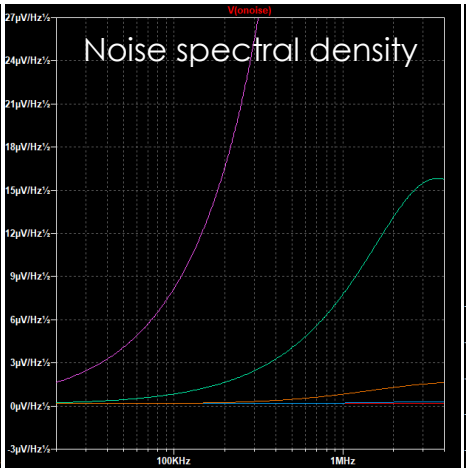
Equivalent circuit with key elements:

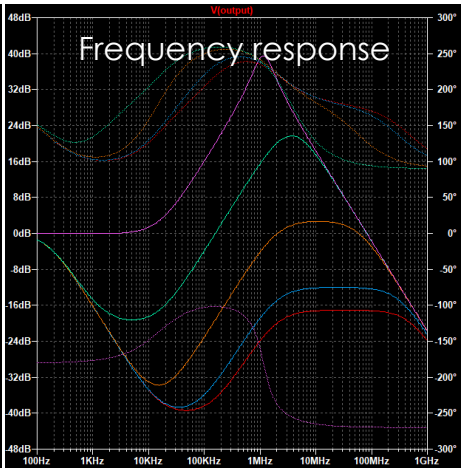
- HV source.
- Return paths circuit - part of the module circuit that stabilizes SMX grounding and suppresses noise from voltage sources (ASIC frequency window 1kHz - 10MHz).
- Sensor strip.
- Micro-cable line.
- STSXYTER channel: opamp with RC feedback, fast shaper, slow shaper.



Simplified schematics of a single detector channel





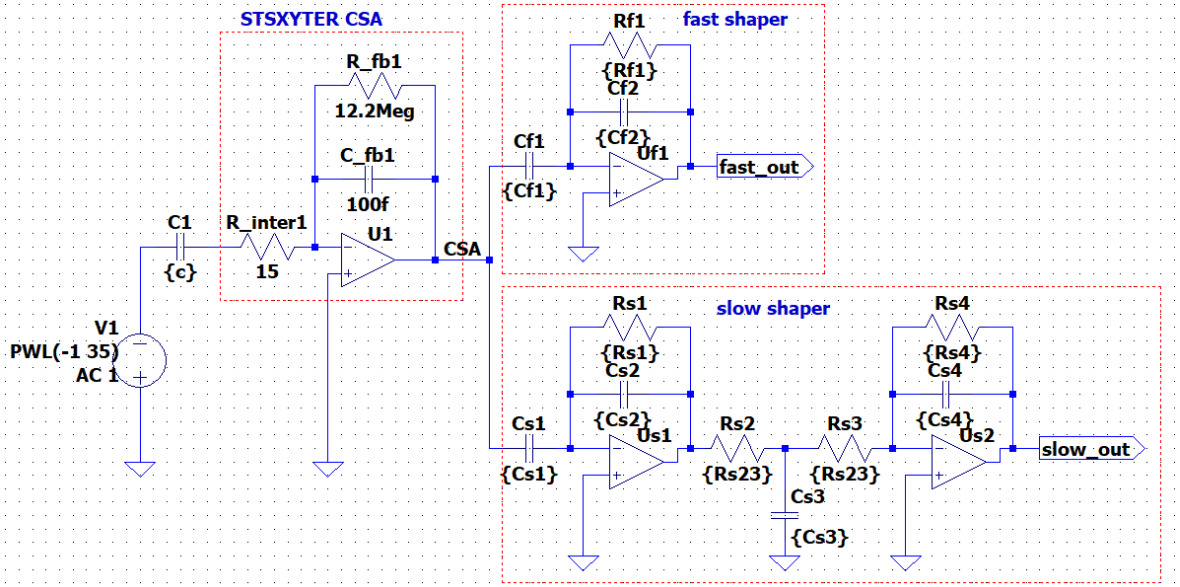


Decimal scan of the values of C_cable1 from 0.1pF to 1µF.

Electronic simulations of the STS module
The noise dependence on capacitive load. Signal's waveform

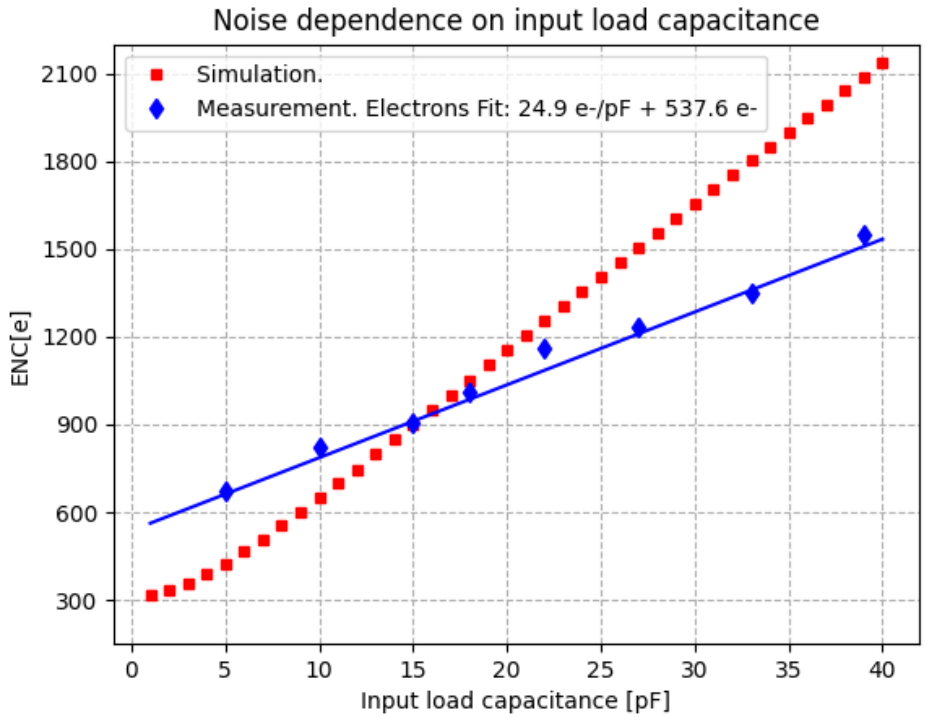
To reproduce the results of the measurement of the noise level and signal waveform as a function of the load capacitance, the next schematic was used:

- V1 - HV source.
- C1 – load capacitance [1-40] pF.
- CSA.
- Fast shaper with shaping time 30 ns.
- Slow shaper with shaping time 90 ns.

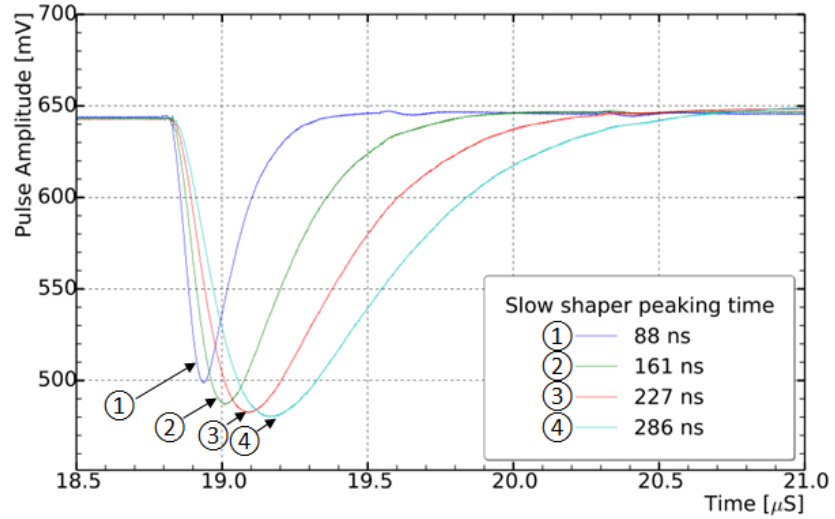


Schematic used for the load capacitance dependence simulation.

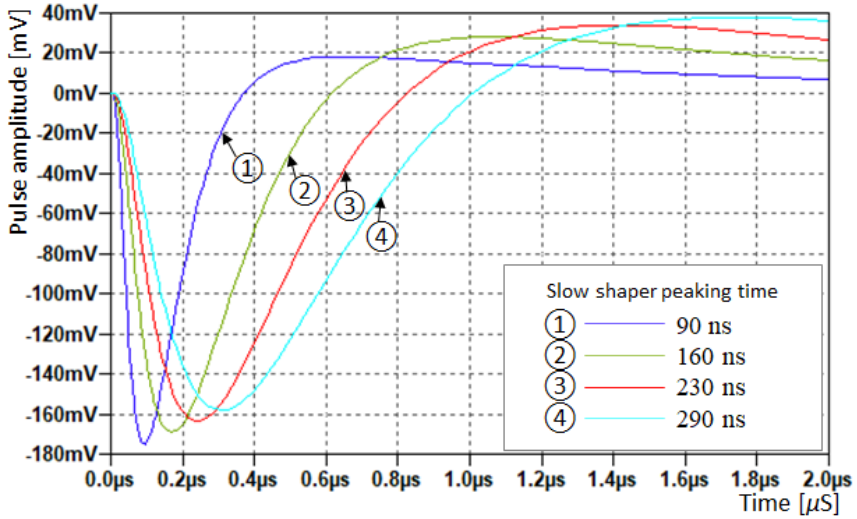
Electronic simulations of the STS module
The noise dependence on capacitive load. Signal's waveform



Noise level at the output of the slow shaper as a function of the load capacitance: measured data (blue), simulated data (red).



Wavaforms of shapers measured at 8 fC for different shaping times



Wavaforms of shapers simulated at 8 fC for different shaping times

Electronic simulations of the STS module
Higher level building blocks

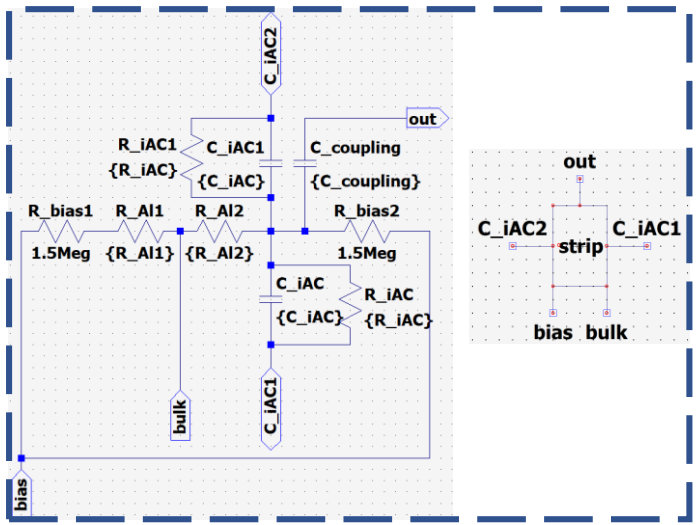
To account for parasitic effects between elements the **multichannel schematic** is needed.

For this purpose and for optimization of multichannel schematic simulation, **custom components were created**:

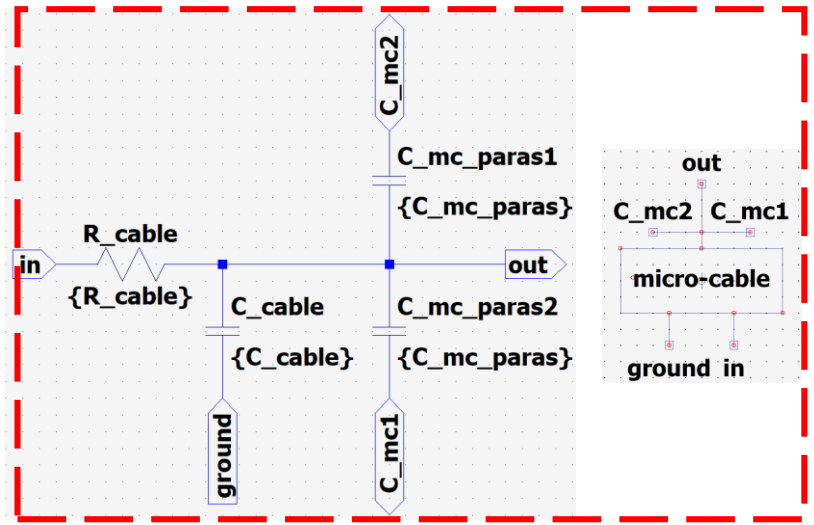
- Strip,
- Micro-cable,
- SMX channel.

Nominal values are parametrized as function of strip or micro-cable **length**.

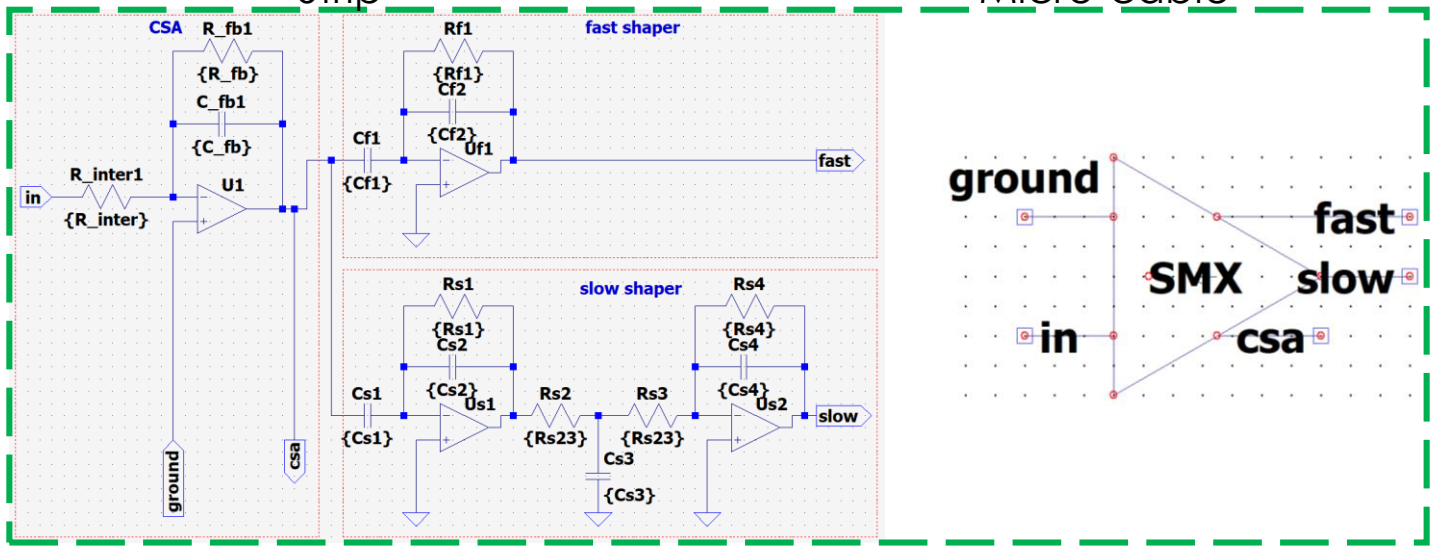
Addition capacitors were added to represent parasitic capacitances between strips and micro-cables.



Strip

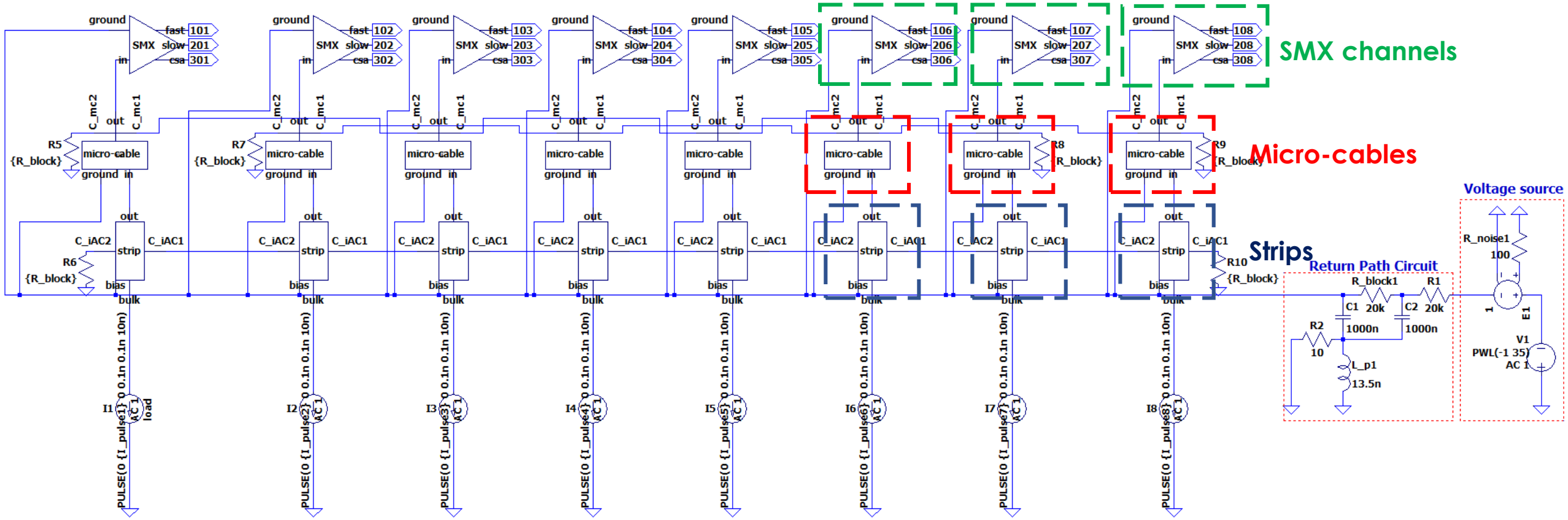


Micro-cable



SMX channel

Electronic simulations of the STS module
Multi-channel schematic. Example of the 8-channel schematic



Using custom components, an 8 channels schematic was assembled to:

- Study the influence of parasitic effects,
- Study the influence of the disconnected or defective strips.

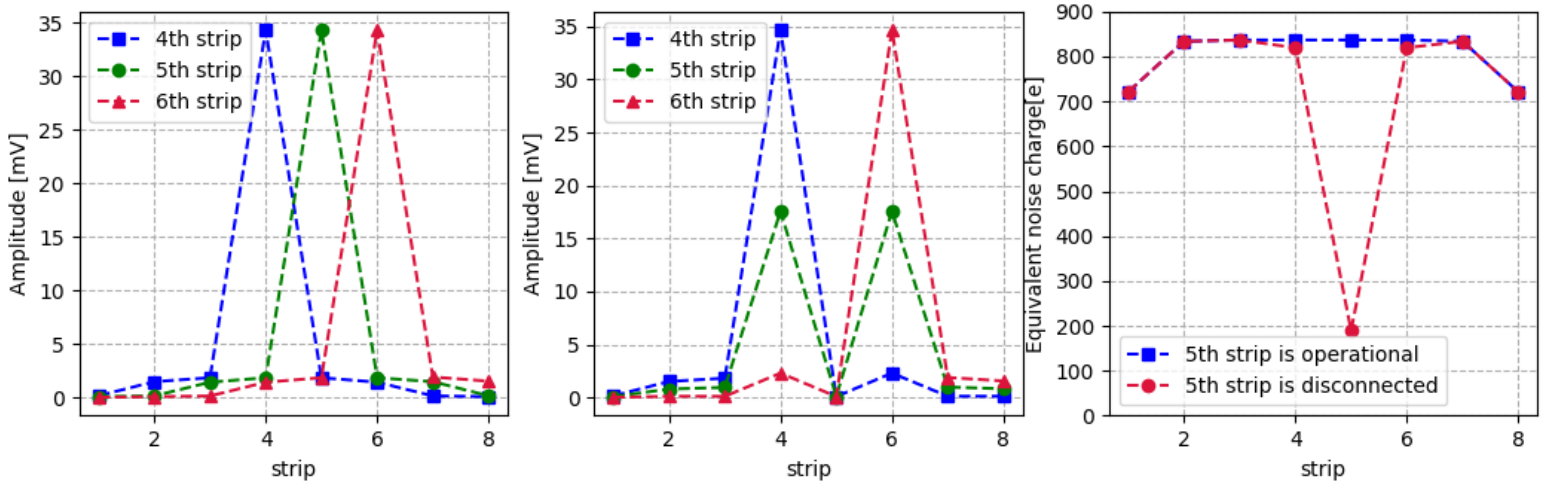
Electronic simulations of the STS module
Multi-channel schematic. Disconnected strips

For all simulations:

- **only 5th strip was disconnected**,
- **signal was sequentially injected on the 4th, 5th, and 6th strips,**
- Signal amplitude and noise level were **measured on the CSA's output of each channel**.

These simulations provide us with:

- **Understanding of importance of the parasitic effects,**
- Approximate **number of channels** needed to adequately describe such effects **without simulating full module**.



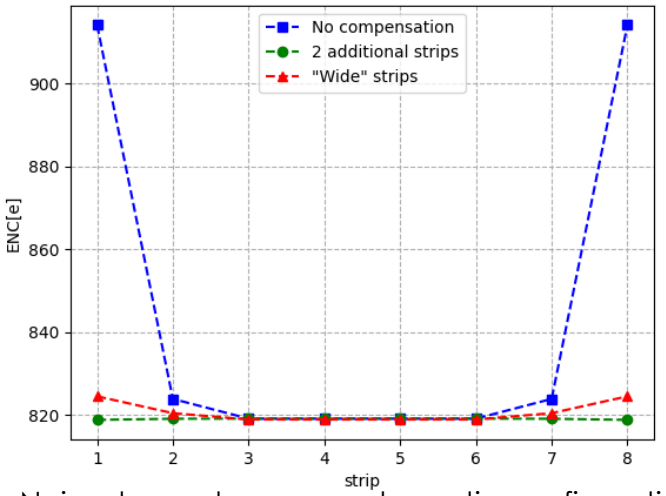
- Connected strip - a single peak.
- Disconnected strip – two picks on adjacent channels (each roughly half of the initial peak).

Opportunity to improve efficiency of the event reconstruction in case of broken channels.

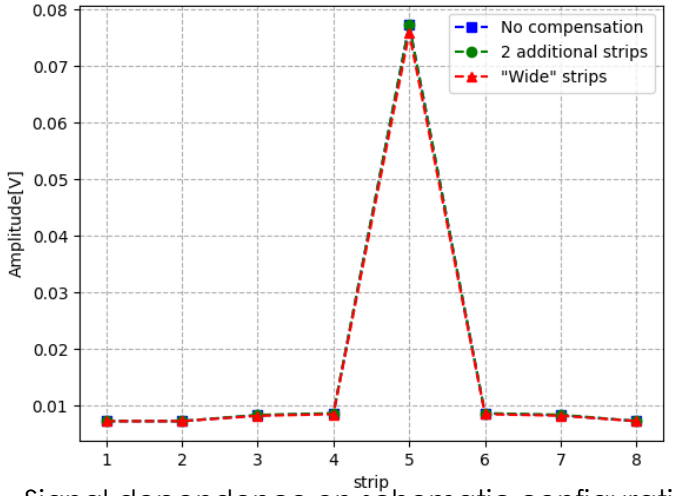
- Significant noise level drops for the disconnected strip.

Identification of the broken strips during the assembly.

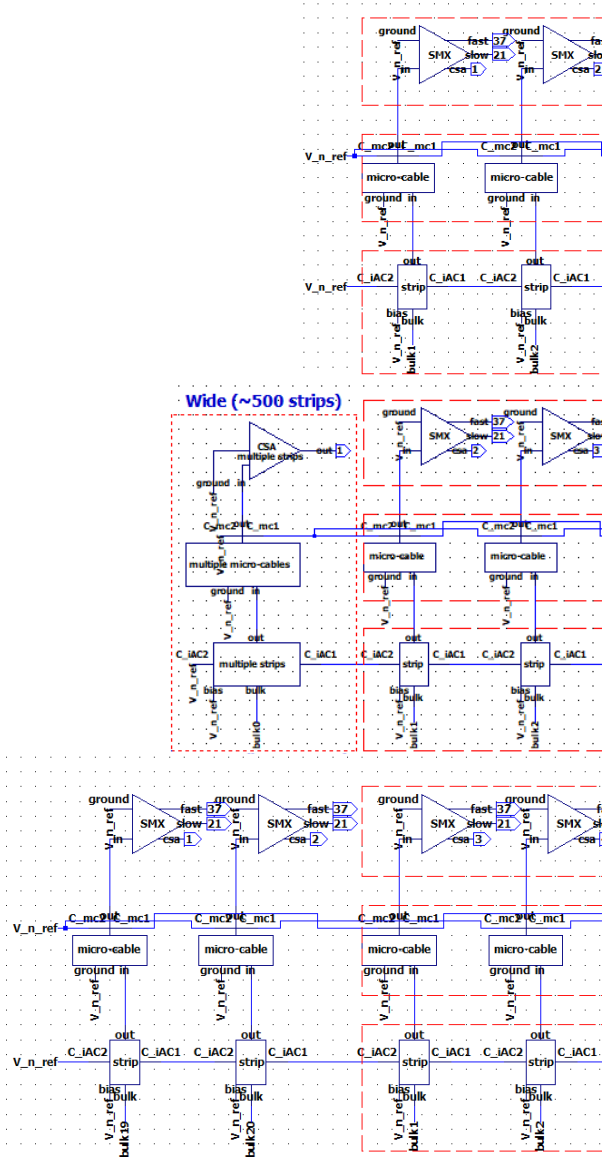
Electronic simulations of the STS module
Multi-channel schematic. Uniform noise level



Noise dependence on schematic configuration



Signal dependence on schematic configuration

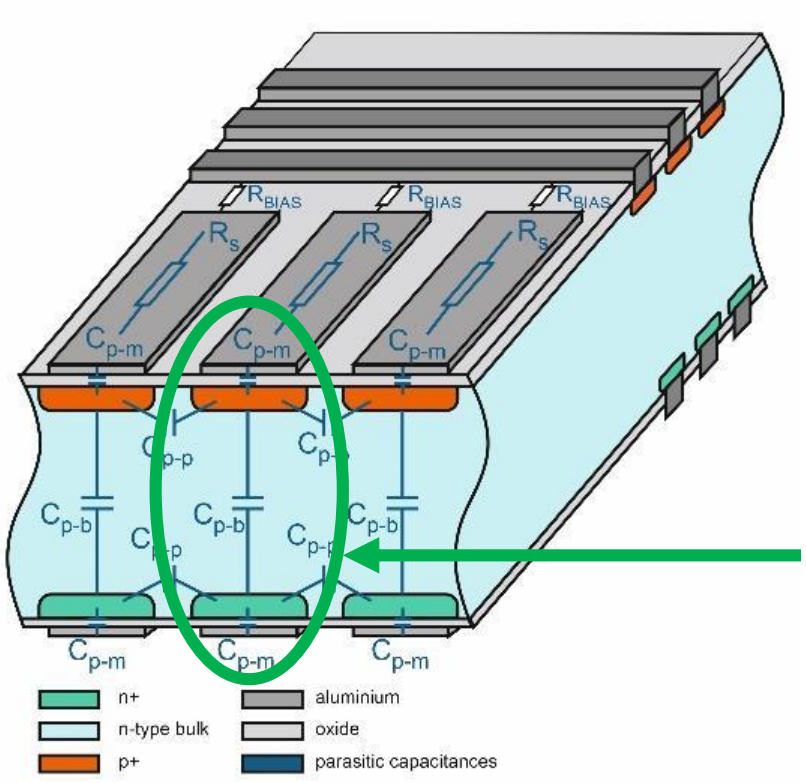


Standard schematic.

Additional high capacitance, low resistance element ("wide" channel).

Two additional compensational channels (2 additional channels).

Electronic simulations of the STS module
Double sided schematic. Parasitic capacitances



Cross-section and parasitic capacitances of double-sided detector.

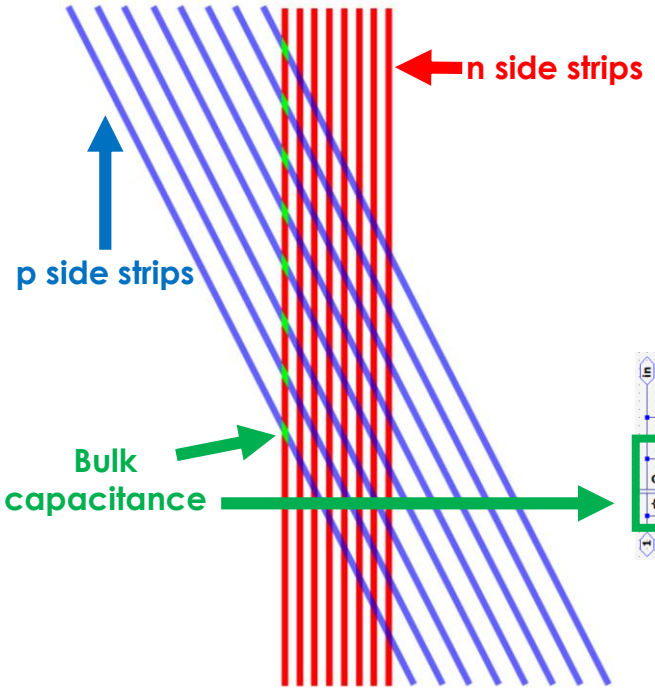
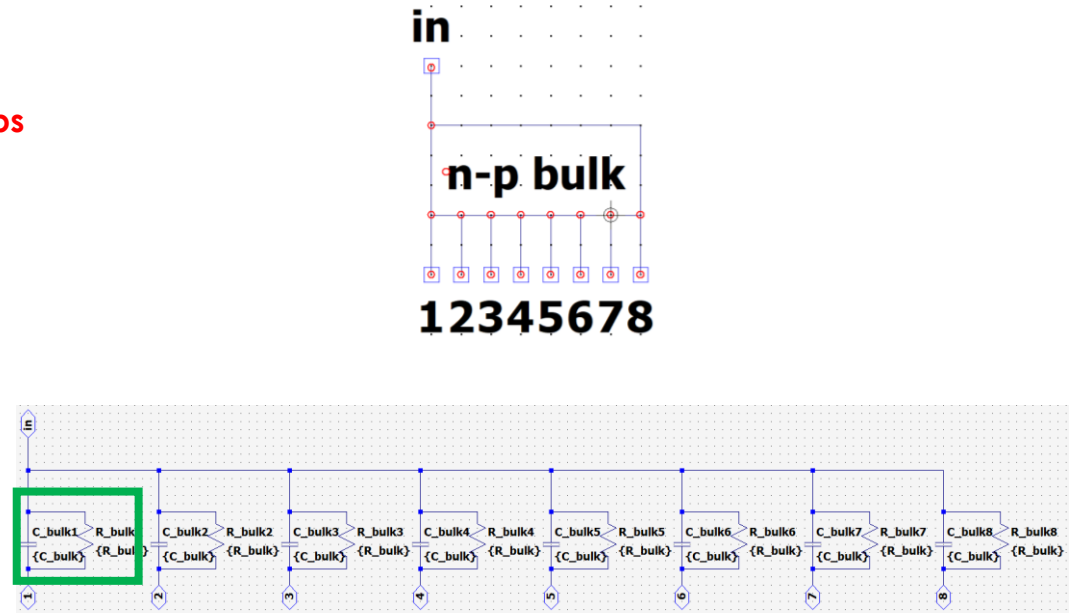
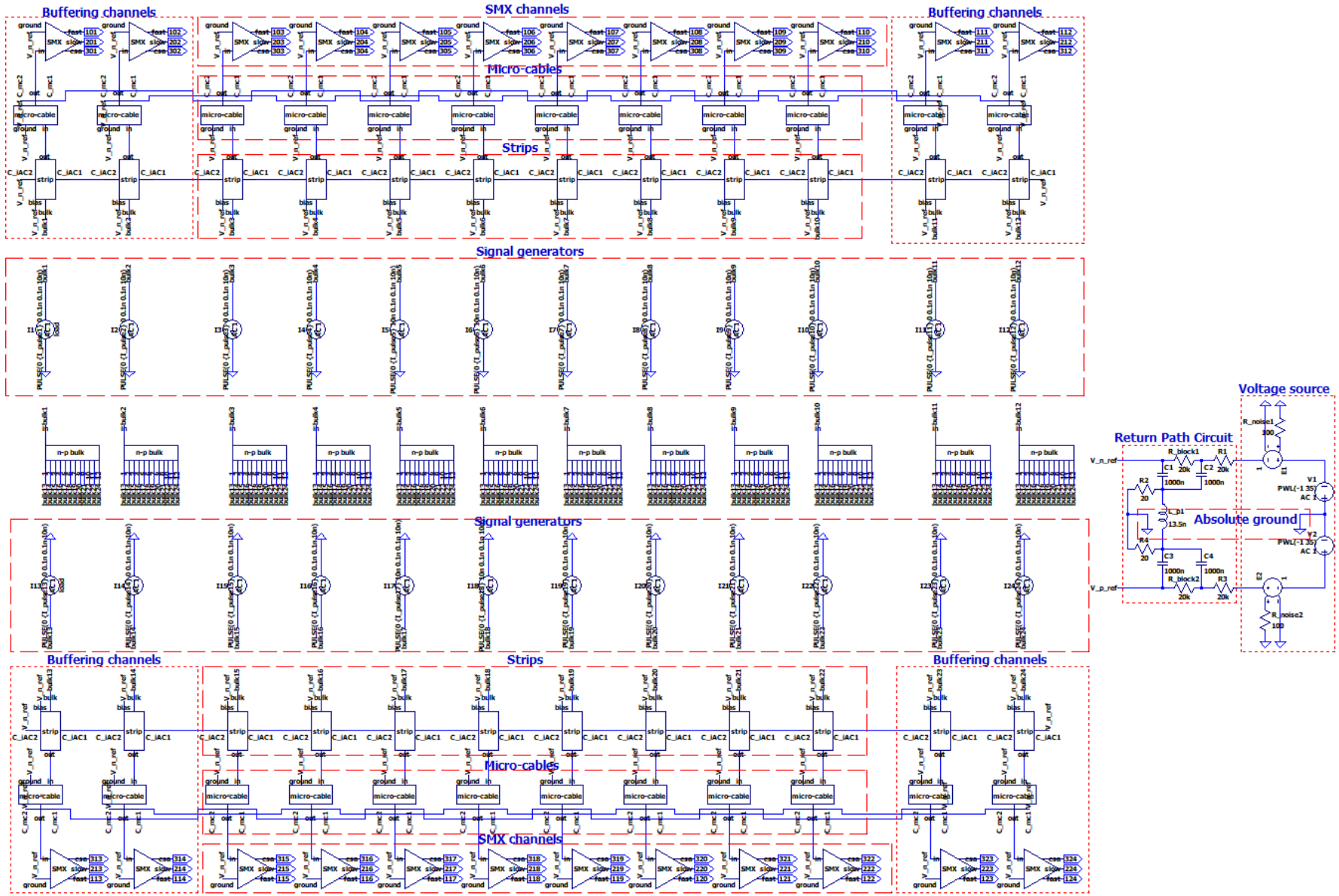


Diagram of the 16-strip schematics, with indication of the bulk capacitances between the first n-side strip and p-side strips (no to scale).



Schematic of the bulk capacitances of a single strip for 16-strip schematic.

Electronic simulations of the STS module. Current schematic

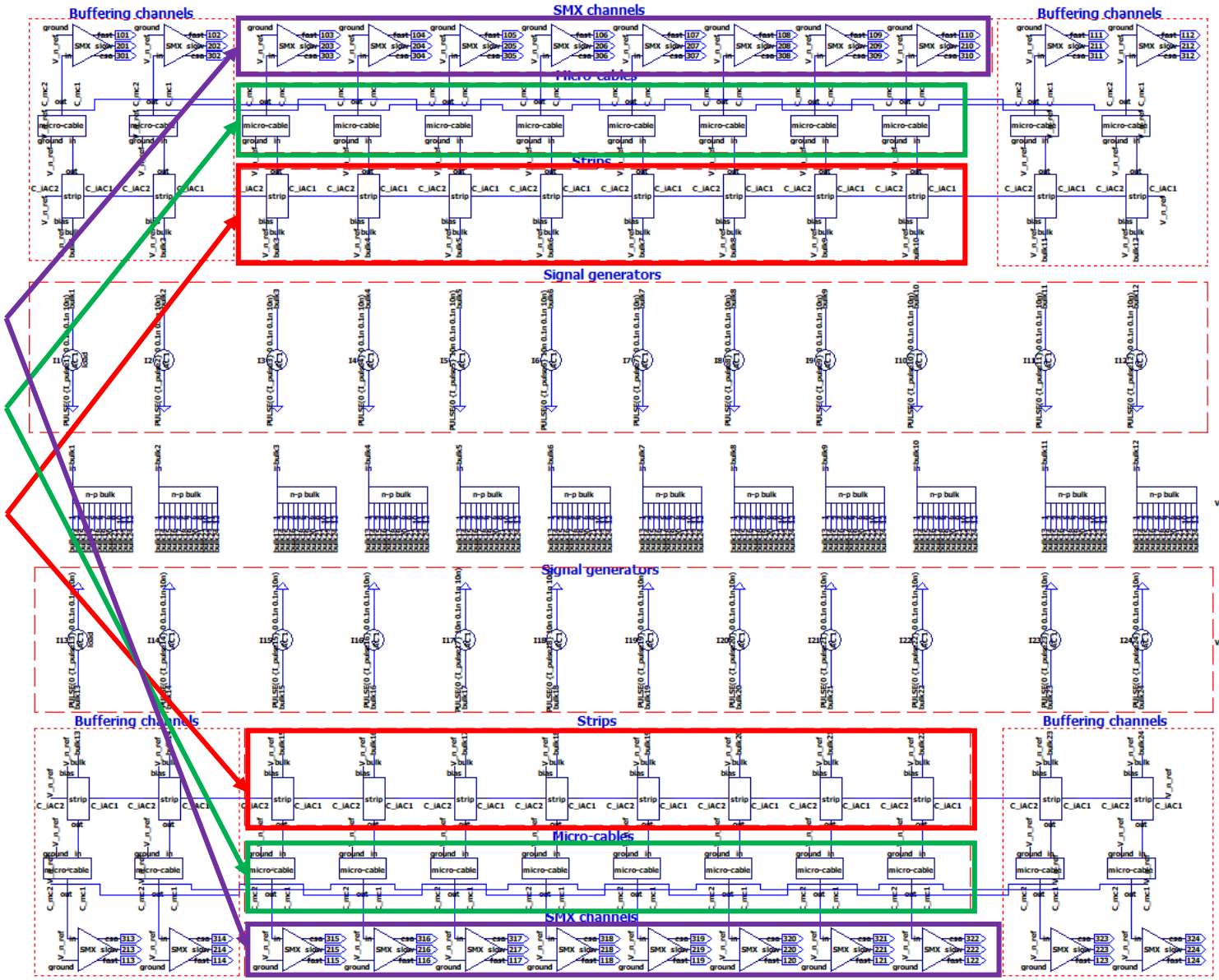


Electronic simulations of the STS module. Current schematic

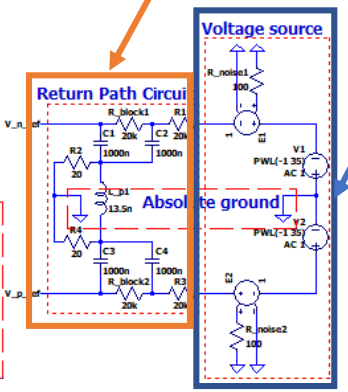
SMX channels

Micro-cables

Strips



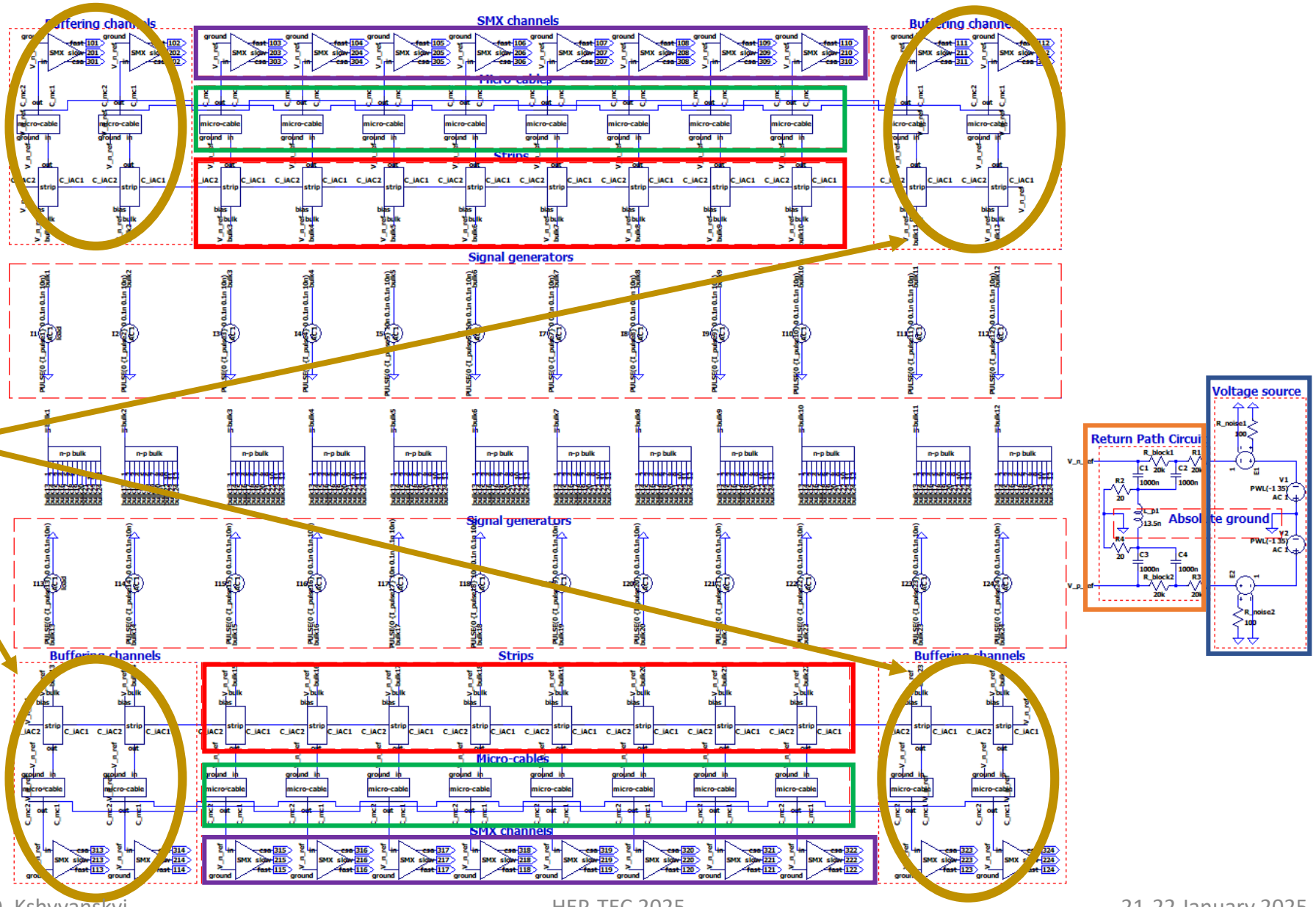
Return Paths Circuit



Voltage source

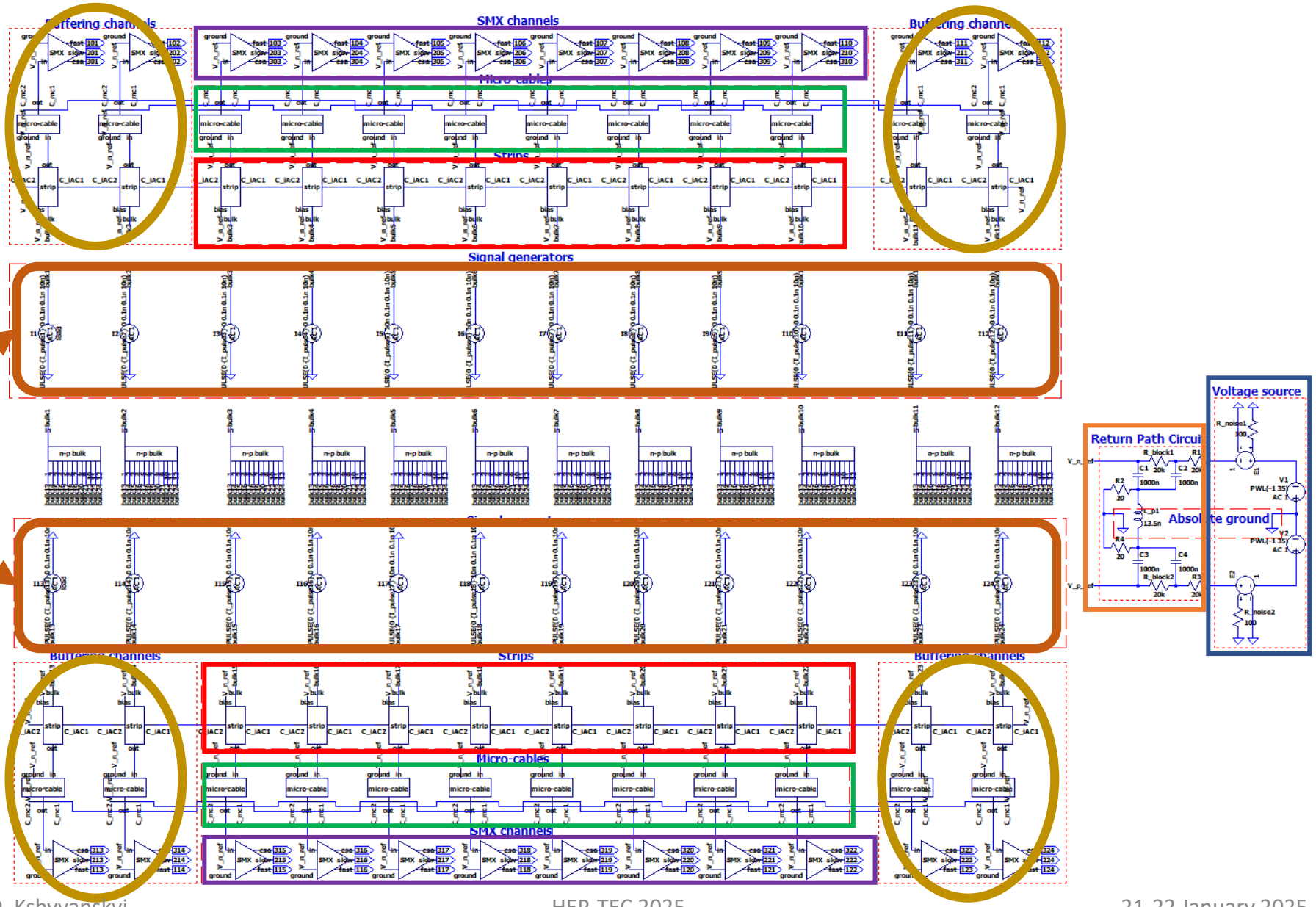
Electronic simulations of the STS module. Current schematic

Noise compensation channels



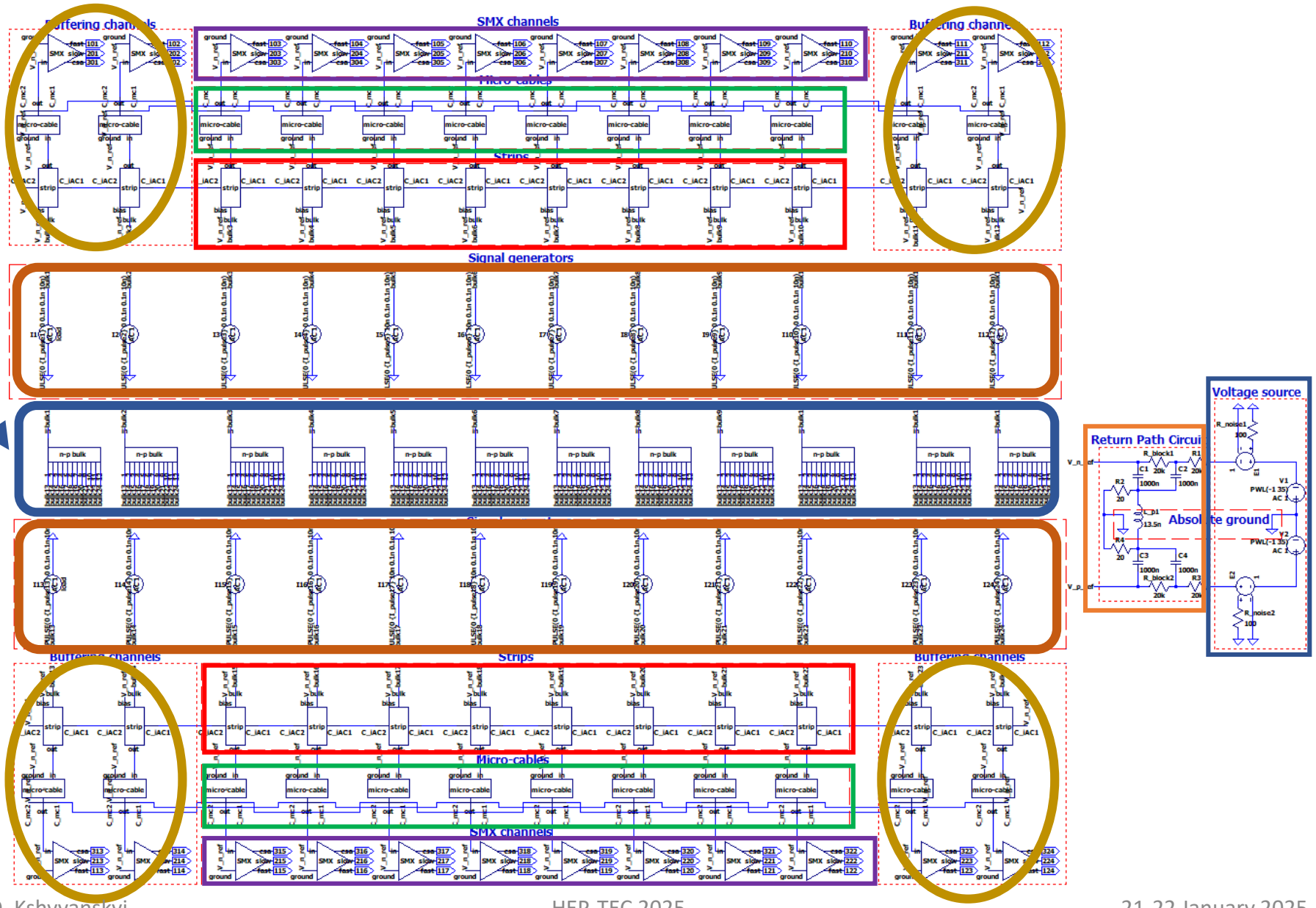
Electronic simulations of the STS module. Current schematic

Signal generators



Electronic simulations of the STS module. Current schematic

Bulk capacitance



Conclusion
Current state of the simulations, furthers plans

- Cross-talk between strips and micro-cables,
- Noise dependence on the length of the components,
- Bulk capacitance,
- Signal oscillation effect.

Plans for further improvement:

- Noise dependence on the capacitive load,
- Shapers waveforms dependence on the injected charge.

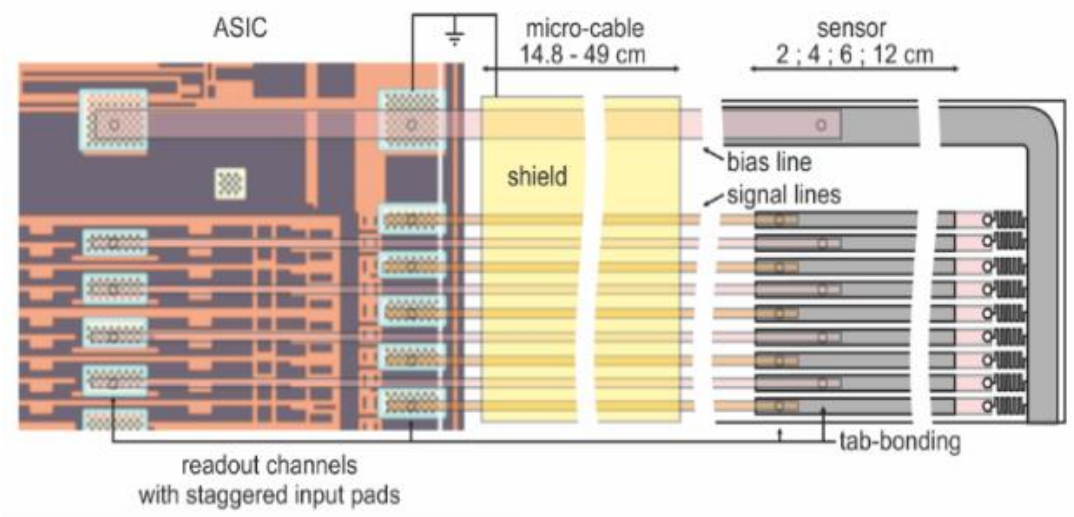
Electronic simulations of the STS module
Results

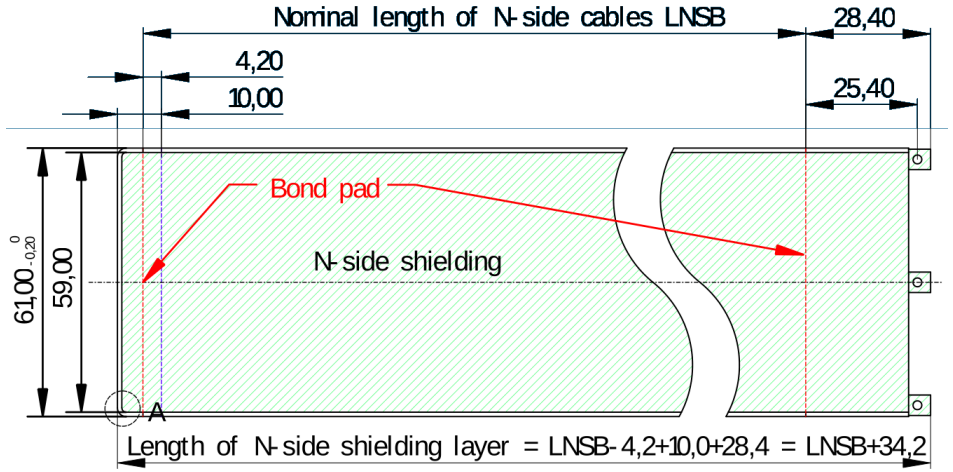
Application of the developed tool

- Improvement of the module quality control,
- Improvement of the reconstruction efficiency,
- Optimization of the detector's working point,
- Optimization of the detector's operational conditions,
- Simulation of the various SMX settings and corresponding detector performance.

Backup slides

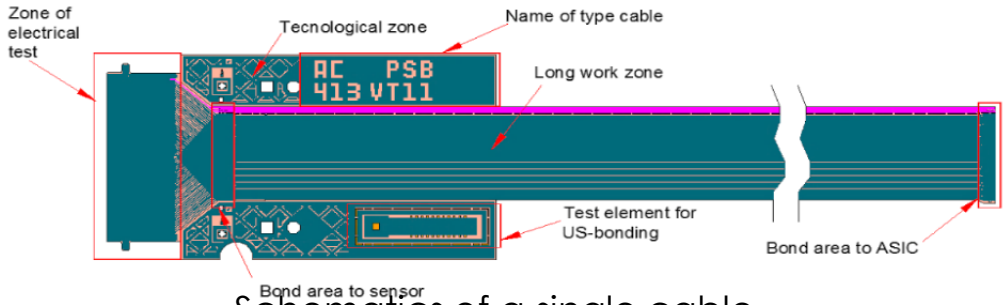
Evaluation of the silicon detector modules. Custom micro-cables





Read-out lines are protected from EMI by aluminium shielding layer.

- **Length from 160mm to 495mm.**
- 2 × 1024 ch./sensor: stack of 32 micro cables per module.



Schematics of a single cable

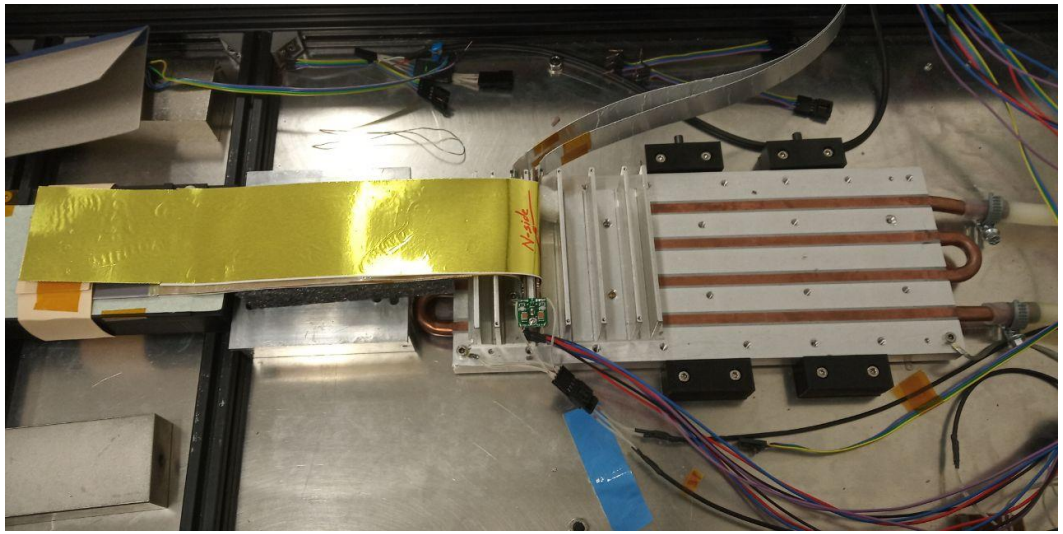
Micro-cable production ongoing at LTU, Kharkiv (60% of ~ 15000 cables ready at GSI)

Evaluation of the silicon detector modules. Module Test Box

Main components:

- Grounded aluminum box.
- One detector module with aluminized polyimide shielding over micro-cable.
- Water cooling system.
- HV and LV interfaces, two data cables from FEBs to CROB.

P-scan (pulse scan) procedure is used to test STS module performance. The charge pulses are generated by inner pulse generator in STS-XYTER.

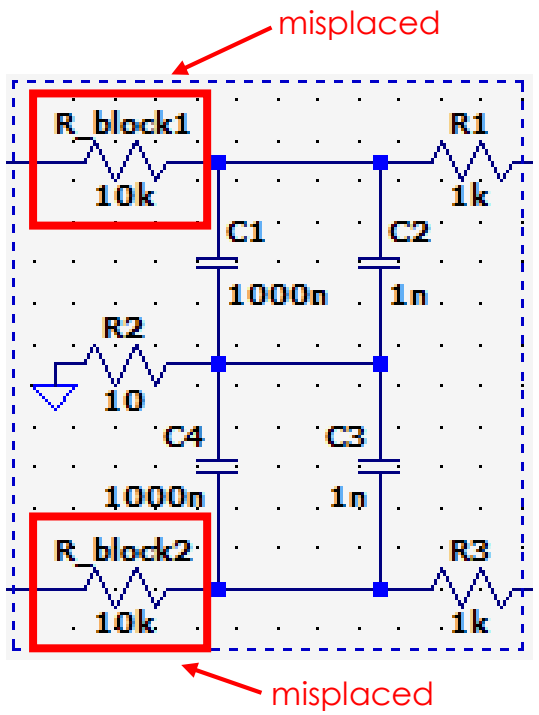


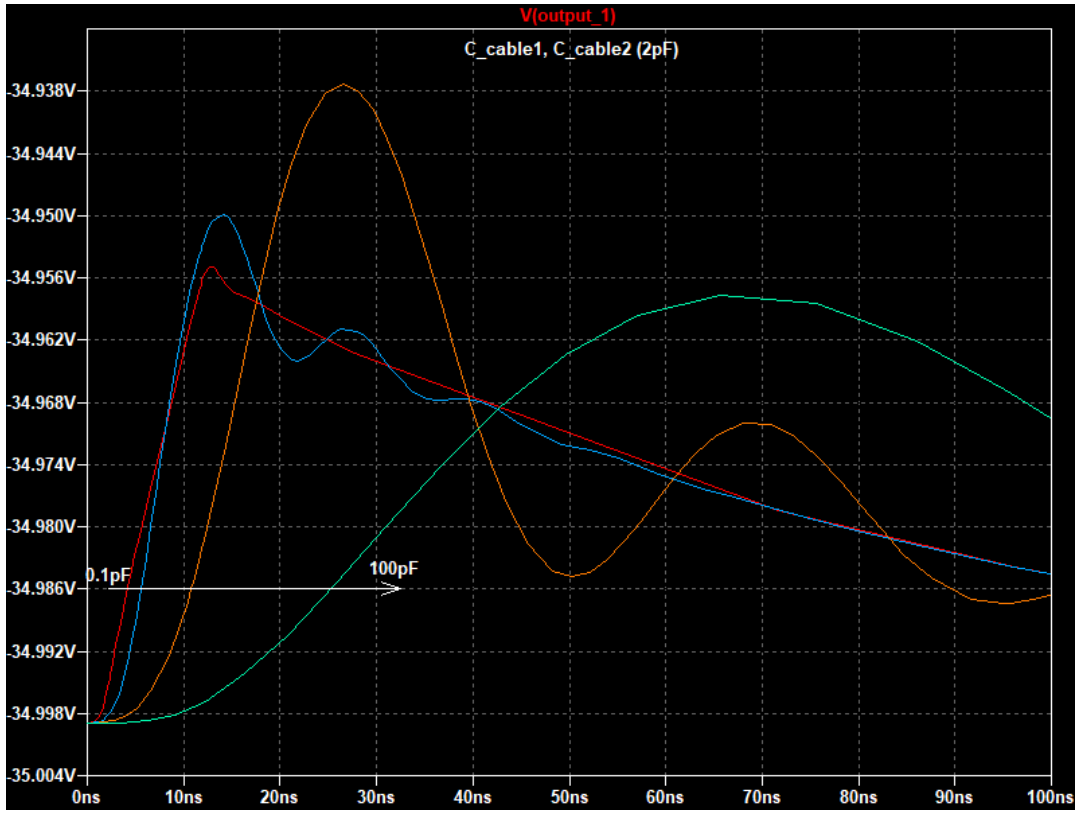
Electronic simulations of the STS module
Signal oscillations

During testing of the return path circuits components' influence, **unexpected oscillations of the output signal** were observed.

Cause – incorrect placement of the R_block components in combination with C_cable being grounded to the same biasing ring.

This gave an insight on a potential cause of oscillations if such ever occur.





Output signal oscillations for C_cable1,2 variations [0.1pF-100pF].